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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,815	03/08/2004	Michael D. Estlick	SUN040063	2783

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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/795,815	ESTLICK ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/15/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/795,815 filed on 3/8/2004.

2. Claims 1-21 have been submitted and examined.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 7/16/2004 is in compliance with 37 CFR 1.97 and 1.98 and is being considered by the examiner. However, the IDS as submitted is not signed. A ***signed*** copy of the IDS previously submitted is required in response to this correspondence.

Specification

4. The disclosure is objected to because of the following informalities:

   a. Page 6, line 14 and 19, "instruction s" should read "instruction"

   b. Page 9, line 7, "permission s" should read "permissions"

   Appropriate correction is required.

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

   c. The term "more significant bit compare" used in claims 1-6, 8-13, and 15-20 is inconsistent with the terminology used in the detailed description of the

specification. The precise meaning of the term is unascertainable from the specification.

d. The term "less significant bit compare" used in claims 1-2, 8-9, and 15-16 is inconsistent with the terminology used in the detailed description of the specification. The precise meaning of the term is unascertainable from the specification.

Claim Objections

6. Claim 20 objected to because of the following informalities:

e. Claim 20 appears to have been intended as a dependent claim, yet there is no mention of which claim it is dependent on. If an independent claim, there would be multiple 35 U.S.C. 112, second paragraph antecedent basis problems. In light of the other independent claims and their dependency trees, the examiner has interpreted that claim 20 is dependent on claim 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. The term "more significant bit compare" in claims 1-6, 8-13, and 15-20 is a relative term which renders the claim indefinite. The term "more significant bit compare" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

It is unknown what constitutes a "more significant" bit compare. What bit does a bit have to be more significant than to be considered "more significant." The term most significant bit (MSB) is common in the art as being the bit position in a binary number having the greatest value, it is a single bit. The use of "more significant bit compare" implies that there is a range involved; a range that has not been defined in the claims or specification. How are the bits more significant, and what are they more significant than?

10. The term "less significant bit compare" in claims 1-2, 8-9, and 15-16 is a relative term which renders the claim indefinite. The term "less significant bit compare" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

It is unknown what constitutes a "less significant" bit compare. What bit does a bit have to be less significant than to be considered "less significant." The term least significant bit (LSB) is common in the art as being the bit position in a binary number having units value, it is a single bit. The use of "less significant bit compare" implies that

there is a range involved; a range that has not been defined in the claims or specification. How are the bits less significant, and what are they less significant than?

11. The terms "low address," "high address", and "mid address" in claims 4, 11, 18 are a relative term which renders the claim indefinite. The terms "low address," "high address", and "mid address" are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

12. Claim 15 recites the limitation "the second compare unit processor" in lines 12-13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 1-2, 4-5, 8-9, 11-12, 15-16, 18-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Pedneau, US patent 6189074 and Watanabe US patent 5109335.

17. With respect to claim 1, Pedneau teaches of a method of performing a fast information compare within a processor comprising: performing a more significant bit compare when information is loaded into a translation lookaside buffer, the more significant bit compare comparing more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information (fig. 8-9; column 7, lines 18-24);

storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information (fig. 8-9; column 7, lines 18-24);

Watanabe teaches of using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and

less significant bits of compare information to determine whether a match is present (fig. 4; column 4, lines 35-51; the comparator compares the TLB result with the output from the LBAA to determine a hit).

It would have been obvious to one of ordinary skill in the art having the teachings of Pedneau and Watanabe at the time of the invention to include the verifying the TLB result with the LBAA as taught in Watanabe in Pedneau. Their motivation would have been to provide high-speed acces and synonym control while reducing power consumption Watanabe (column 2, 30-52).

18. With respect to claim 2, Pedneau teaches of the result of the more significant bit compare is active (fig. 8-9; column 7, lines 18-24; as the address lies within the defined region, it is active)

Watanabe teaches of providing an indication of a match to the compare information when the result of the more significant bit compare is active and the less significant bits of the information match the less significant bits of the compare information (fig. 4; column 4, lines 45-51; as there is a hit from the TLB, the result is active and the bits 47 (less significant) matching with those in LBAA).

19. With respect to claim 8, Pedneau teaches of an apparatus for performing a fast information compare within a processor comprising: means for performing a more significant bit compare when information is loaded into a translation lookaside buffer, the more significant bit compare comparing more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information (fig. 8-9; column 7, lines 18-24);

means for storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information (fig. 8-9; column 7, lines 18-24);

Watanabe teaches of means for using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present (fig. 4; column 4, lines 35-51; the comparator compares the TLB result with the output from the LBAA to determine a hit).

20. With respect to claim 9, Pedneau teaches of the result of the more significant bit compare is active (fig. 8-9; column 7, lines 18-24; as the address lies within the defined region, it is active)

Watanabe teaches of means for providing an indication of a match to the compare information when the result of the more significant bit compare is active and the less significant bits of the information match the less significant bits of the compare information (fig. 4; column 4, lines 45-51; as there is a hit from the TLB, the result is active and the bits 47 (less significant) matching with those in LBAA).

21. With respect to claim 15, Pedneau teaches of a processor comprising: a translation lookaside buffer (fig. 8; item 1009); and

a first compare unit coupled to the translation lookaside buffer (fig. 8, item 1007; column 6, line 21),

the first compare unit performing a more significant bit compare when information is loaded into a translation lookaside buffer, the more significant bit compare comparing

more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information (fig. 8-9; column 6, lines 21-26, column 7, lines 18-24),

the first compare unit storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information (fig. 8-9; column 7, lines 18-24);

Watanabe teaches of a second compare unit coupled to the translation lookaside buffer (fig. 4, item 8),

the second compare unit processor using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present (fig. 4; column 4, lines 35-51; the comparator compares the TLB result with the output from the LBAA to determine a hit).

22. With respect to claim 16, Pedneau teaches of the result of the more significant bit compare is active (fig. 8-9; column 7, lines 18-24; as the address lies within the defined region, it is active)

Watanabe teaches of wherein: the second compare unit provides an indication of a match to the compare information when the result of the more significant bit compare is active and the less significant bits of the information match the less significant bits of the compare information (fig. 4; column 4, lines 45-51; as there is a hit from the TLB, the result is active and the bits 47 (less significant) matching with those in LBAA).

23. With respect to claims 4, 11, and 18, Pedneau teaches of wherein: the compare information corresponds to sample selection criteria; and the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria (fig. 8-9; column 4, lines 25-35, column 6, lines 21-26, column 7, lines 18-24; the address range comprises selection criteria).

24. With respect to claims 5, 12, and 19, Pedneau teaches of wherein: the sample selection criteria includes a sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address (column 4, lines 25-35; as there is an address range, there upper and lower address bounds and addresses between them); and the result of the more significant bit compare indicates whether the more significant bits of the information being loaded correspond one of a plurality of conditions indicated by the sample selection criteria (fig. 8-9; column 4, lines 25-35, column 6, lines 21-26, column 7, lines 18-24).

25. Claims 3, 10, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedneau and Watanabe as applied to claims 1, 8, and 15 respectively, and further in view of SPARC Joint Programming Specification (JPS1): Commonality (manual).

26. With respect to claims 3, 10, and 17, the manual teaches of wherein: compare information corresponds to a virtual address watchpoint (pages 94-96); and

the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address (pages 94-96).

It would have been obvious to one of ordinary skill in the art having the teachings of Pedneau, Watanabe and the manual at the time of the invention to include the watchpoint registers in the combination of Pedneau and Watanabe as taught in the manual. Their motivation would have been to allow for efficient debugging of processes.

27. Claims 6, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedneau and Watanabe as applied to claims 1, 8, and 15 respectively, and further in view of Akkary et al. US patent 5671444.

28. With respect to claims 6, 13, and 20 Akkary teaches of wherein: the processor includes a memory management unit including a memory management unit translation lookaside buffer (fig. 2, items 14, 25, 28) and

an instruction fetch unit including an instruction translation lookaside buffer (fig. 2, items 12, 18; items 12 and 18 comprise an instruction fetch unit); and

It would have been obvious to one of ordinary skill in the art having the teachings of Pedneau, Watanabe, and Akkary at the time of the invention to include an instruction fetch unit, memory management unit, and duplicating the TLB creating an instruction TLB and a data TLB in the combination of Pedneau, and Watanabe as taught in Akkary. Their motivation would have been to allow the processor to run more efficiently as it would not have instructions stalling when a data lookup in the TLB is carried out since they are separate.

In the combination of Pedneau, Watanabe, and Akkary, the more significant bit compare is performed when information is loaded into the instruction translation lookaside buffer as it is done in both TLBs.

29. Claims 7, 14, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedneau and Watanabe as applied to claims 1, 8, and 15 respectively, and further in view of Kling, US patent application publication 2004/0049657.

30. With respect to claims 7, 14, 21, Kling teaches of the processor includes a plurality of threads (paragraph 0029); and

the compare information is unique for each of the plurality of threads (paragraph 0029).

It would have been obvious to one of ordinary skill in the art having the teachings of Pedneau, Watanabe and Kling at the time of the invention to implement multiple threads in the processor with each thread having its own page ID or tag in the combination of Pedneau and Watanabe as taught in Kling, thus making the page address ranges separate for each thread in the combination of Pedneau and Watanabe. Their motivation would have been to allow the processor to operate quicker with more threads and to avoid conflicts between threads by keeping their pages separate (paragraph 0029).

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael C. Krofcheck

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